

EAST - [10691240.wsp:1]

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L1: (1) (ball near grid near array or BGA) and packag\$3 and (fold\$3 with substrate) and
L2: (1) (ball near grid near array or BGA) and packag\$3 and (fold\$3 with substrate) and
L3: (1) (ball near grid near array or BGA) and (fold\$3 with substrate) and pad near oper
L4: (44) (ball near grid near array or BGA) and (fold\$3 with substrate) and opening
L5: (54) (ball near grid near array or BGA) and pad near opening and coat\$3
Failed
Saved
(22984) (ball near grid near array or BGA) nad packag\$3 and fold\$3 with substrate
(21268) (ball near grid near array or BGA) nad packag\$3 and fold\$3 near substrate
(55) (ball near grid near array or BGA) and packag\$3 and fold\$3 near substrate
(97) (ball near grid near array or BGA) and packag\$3 and (fold\$3 with substrate)
(0) 4 and stack\$3
(67) (ball near grid near array or BGA) and packag\$3 and (fold\$3 with substrate) and st
(460) fold\$3 near substrate and packag\$3
(184) fold\$3 near substrate and packag\$3 and stack\$3
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Default operator: ☒ Highlight all hit terms initially

(ball near grid near array or BGA) and pad near opening and coat\$3

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|----|--------------------------|--------------------------|---------------|------------|-------|---|------------|--------------------------|
| 30 | <input type="checkbox"/> | <input type="checkbox"/> | US 6667439 B2 | 20031223 | 12 | Integrated circuit package including opening exposing portion of an IC | 174/52.1 | 257/690; 257/787; |
| 31 | <input type="checkbox"/> | <input type="checkbox"/> | US 6653742 B1 | 20031125 | 60 | Semiconductor chip assembly with interlocked conductive trace | 257/783 | 156/292; 156/307.3; |
| 32 | <input type="checkbox"/> | <input type="checkbox"/> | US 6649961 B2 | 20031118 | 27 | Supporting gate contacts over source region on MOSFET devices | 257/296 | 257/401; 257/673; |
| 33 | <input type="checkbox"/> | <input type="checkbox"/> | US 6617655 B1 | 20030909 | 22 | MOSFET device with multiple gate contacts offset from gate contact area and over | 257/401 | 257/737; 257/738; |
| 34 | <input type="checkbox"/> | <input type="checkbox"/> | US 6608374 B1 | 20030819 | 55 | Semiconductor chip assembly with bumped conductive trace | 257/690 | 257/E21.508 |
| 35 | <input type="checkbox"/> | <input type="checkbox"/> | US 6593220 B1 | 20030715 | 13 | Elastomer plating mask sealed wafer level package method | 438/612 | 228/180.22; 438/613; |
| 36 | <input type="checkbox"/> | <input type="checkbox"/> | US 6586682 B2 | 20030701 | 14 | Printed wiring board with controlled line impedance | 174/255 | 361/795 |
| 37 | <input type="checkbox"/> | <input type="checkbox"/> | US 6576539 B1 | 20030610 | 61 | Semiconductor chip assembly with interlocked conductive trace | 438/611 | 257/E21.508; 438/110; |
| 38 | <input type="checkbox"/> | <input type="checkbox"/> | US 6576493 B1 | 20030610 | 48 | Method of connecting a conductive trace and an insulative base to a semiconductor | 438/107 | 257/E21.508 |
| 39 | <input type="checkbox"/> | <input type="checkbox"/> | US 6548393 B1 | 20030415 | 28 | Semiconductor chip assembly with hardened connection joint | 438/618 | 257/693; 257/778; |
| 40 | <input type="checkbox"/> | <input type="checkbox"/> | US 6543128 B2 | 20030408 | 10 | Ball grid array package and its fabricating process | 29/841 | 257/E23.069 |